A Technique for Improving the Distortion of GaAs Variable Attenuator IC Using Squeezed-Gate FET Structure

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Abstract

This paper describes a novel technique for improving the distortion of the GaAs attenuator IC using squeezed-gate structure of MESFETs. We found that the distortion was originated from the steep cutoff Id-Vgs curve of conventional FETs. To obtain smooth cutoff characteristics, we devised the squeezed-gate structure where the FETs with different threshold voltages are connected in parallel making use of the short channel effect. Fabricated IC shows 10 dB reduction of the 3rd order intermodulation distortion by optimizing the ratio of the gate widths.

Introduction

There has been a growing demand for RF variable attenuators to control transmitting power of the digital cellular phones. Such attenuators are placed at the input of the power amplifier to reduce excess power consumption when the base station is near by. Although monolithic GaAs attenuator IC has an advantage of almost zero power dissipation and small package size [1-4], it shows a quite large distortion which seriously degrades the bit error rate.

In this paper, we report on a novel technique for improving the distortion of the GaAs attenuator IC using squeezed-gate structure of MESFETs. We found that the distortion was originated from the steep cutoff Id-Vgs curve of conventional FETs. To obtain smooth cutoff characteristics, we devised the squeezed-gate structure where the FETs with different threshold voltages are connected in parallel making use of the short channel effect. Fabricated IC shows 10 dB reduction of the 3rd order intermodulation distortion by optimizing the ratio of the gate widths.

Squeezed-Gate FET

Conventional GaAs FET used as variable impedance device is designed to have low on-resistance to obtain low insertion loss. Such a FET shows a steep Id-Vgs curve as shown in Fig. 1(a). This steep cutoff characteristics causes large distortion especially when the FET is biased at around the threshold voltage. This is because the gate voltage is modulated by the input RF signal due to the parasitic capacitances Cgd or Cgs. The FET with deeper threshold voltage and smaller gate width shows a low-pitched cutoff characteristics (Fig. 1 (b)), however, the on-resistance is increased resulting in degrading the insertion loss. The parallel connection of these two FETs will show smooth cutoff characteristics without increasing the on-resistance as shown in Fig. 1 (c).

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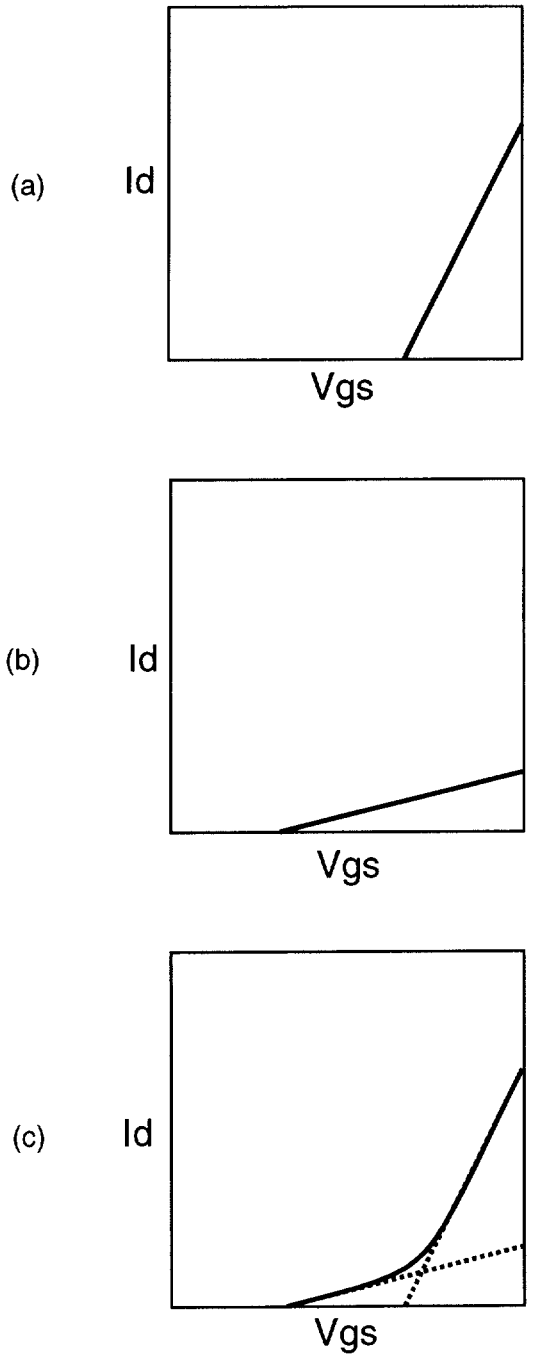

Figure1. Schematic of the Id-Vgs charateristics.
(a) conventional FET.
(b) FET with deeper threshold voltage.
(c) parallel connection of (a) and (b).

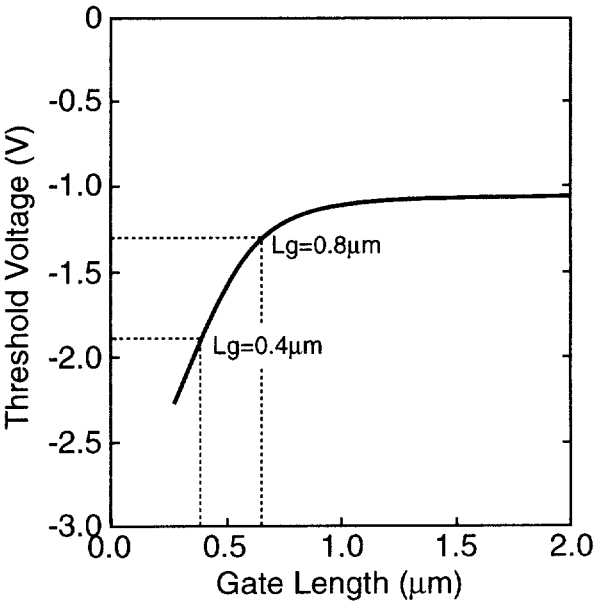

Figure2. An Example of the short channel effect of the GaAs MESFET.

As well-known, there exists the short channel effect of the GaAs MESFET as shown in Fig. 2. Utilizing this short channel effect, we devised the squeezed-gate FET structure as shown in Fig. 3 (a). This configuration is equivalent to the parallel connection of FETs that have two different threshold voltages(Fig. 3 (b)). It should be noted that this favorable characteristics is obtainable only by mask layout of the gate patterning without using complicated epi structure or fabrication process.

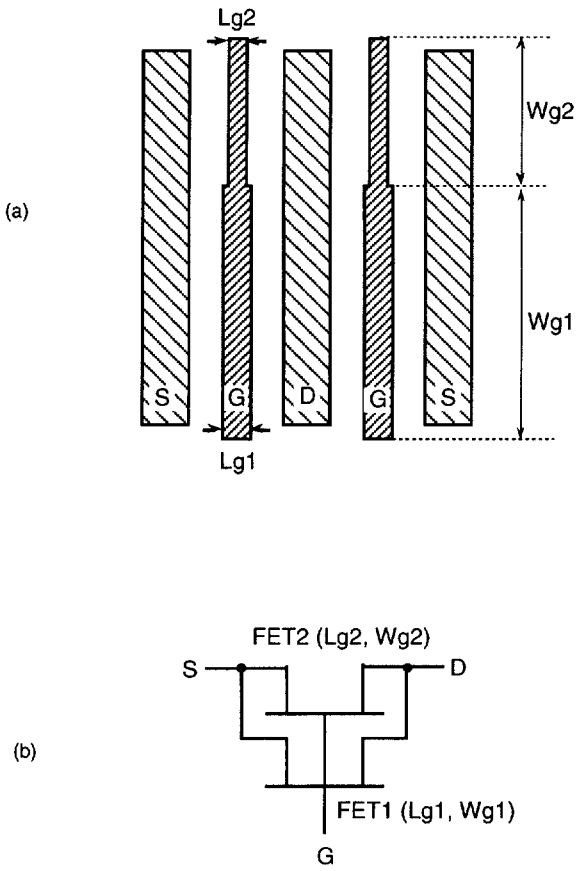

Figure 3. Schematic of the squeezed-gate FET structure (a) and its equivalent circuit(b) .

The chip photograph is shown in Fig. 5. The chip size is 0.58 mm x 0.7 mm. The lengths of the squeezed-gate (Lg1 and Lg2 in Fig. 1 (a)) are 0.4 and 0.8 μm. The total gate width (Wg1 + Wg2) of each FET is 1.2 mm.

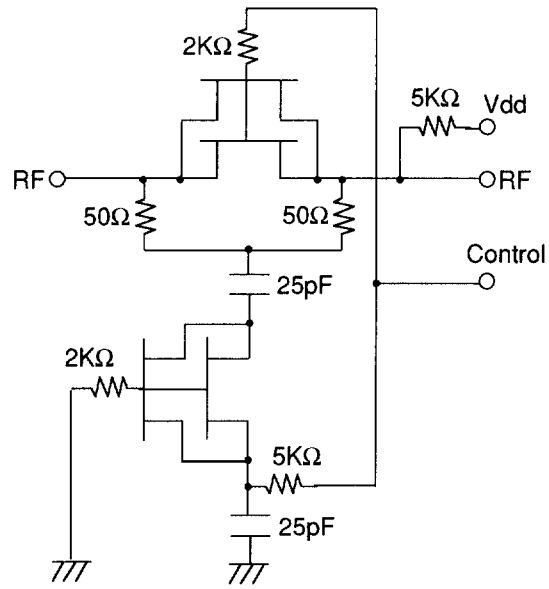

Figure 4. Designed variable attenuator circuit using squeezed-gate FETs.

Attenuator IC Fabrication

To confirm the improvement of the distortion by the squeezed-gate structure, we designed and fabricated attenuator IC. Figure 4 shows the designed variable attenuator circuit using the squeezed-gate FET's. Two capacitors as large as 25pF enable this bridged-T type attenuator circuit to operate with a single positive control voltage.[4,5]. To integrate such large capacitors on a GaAs substrate, on-chip BST (Barium Strontium Titanate) capacitor technology [6-7] was employed.

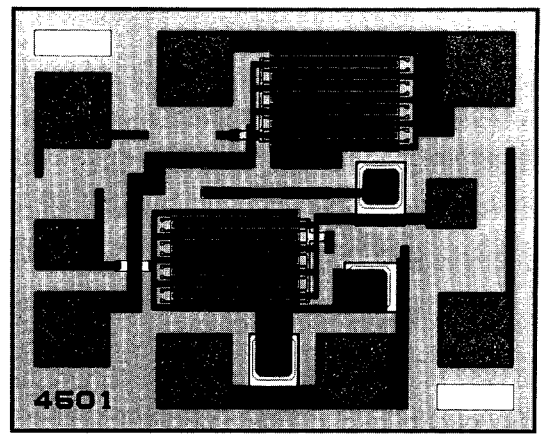

Figure 5. Chip micro photograph of the fabricated attenuator IC

Measurement Result

The 3rd order intermodulation distortion (IM3) of the fabricated IC was measured by using the 2-tone method. Figure 6 shows the measured IM3 as a function of the ratio of the width of the squeezed-gate. The IM3 shows a minimum value of -31dBc at the gate-width ratio of 0.35. This value is 10dB lower than that of the conventional constant gate-length FET.

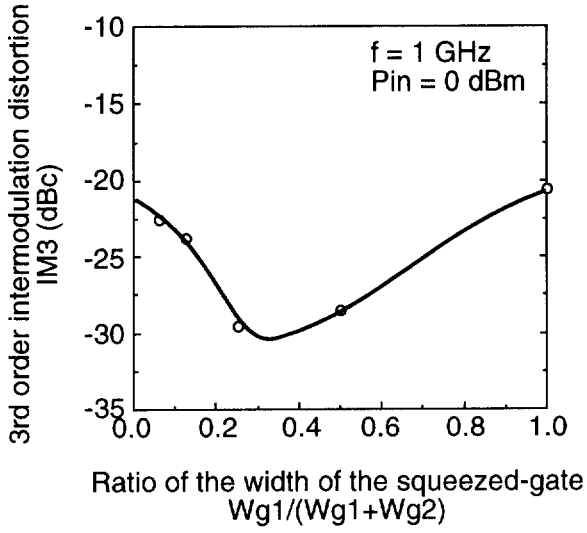

Figure 6. The 3rd order intermodulation distortion (IM3) of the fabricated IC as a function of the width ratio of the squeezed gate.

Conclusion

We have developed a novel technique for improving the distortion of the GaAs attenuator IC using squeezed-gate structure of MESFETs, where two different length of the gates are connected in each finger. Owing to the smooth cutoff characteristics of the Id-Vgs curve, the 3rd order intermodulation distortion shows 10 dB improvement from the conventional FET structure. This technique contributes to design of low-distortion GaAs attenuator IC for digital mobile communication systems such as TDMA or CDMA.

Acknowledgement

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